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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,238	04/20/2005	Kazutoshi Nakajima	046124-5303	7461

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EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,238	NAKAJIMA, KAZUTOSHI	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/20/05,4/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: the language recites "the lower step surface being located between the upper step surface and the middle step surface", which contradicts the notion of "the lower step". The claim is interpreted to mean that the lower step surface is between the upper step surface and the middle step surface *in a lateral direction*.

2. Claim 3 is objected to because of the following informalities: the language "a ramp portion consisting of a level difference between the upper step surface and the lower step surface" is believed to be in error. The language should read: "a ramp portion consisting of a level difference between the upper step surface and the middle step surface" as recited on page 13 of the specification (in Fig 1B, the upper step is 2u, the middle step is 2m, the lower step is 2d). It is noted that claim 3 is not in error if the informalities of claim 1 are not corrected (according to claim 1, item 2m may be "the lower step"). Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **1-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hisahiro (JP 61,171,176) and Hisahiro (JP 60,163,471).

5. Regarding claim **1**, the '176 document discloses in Fig 1(f) a semiconductor photodetector comprising: a semi-insulating substrate (1) having an upper step surface (top of item 1) and a lower step surface (bottom of item 2) with their respective height different from each other in a top surface portion; a first semiconductor layer (2) formed immediately above the lower step surface and comprising a first impurity (p+); a second semiconductor layer (4) formed above the second top surface portion of the first semiconductor layer, having a top surface portion of a flat surface shape with a height equal to that of the upper step surface (top of item 4 is flush with top of item 1), and comprising a second impurity (n); a first electrode (7) provided astride and above the first top surface portion of the first semiconductor layer; and a second electrode (5) provided astride and above the top surface portion of the second semiconductor layer and the upper step surface of the semi-insulating substrate.

The '176 document fails to specify a middle step surface, the lower step surface being located between the upper step surface and the middle step surface in a lateral direction, where the first layer has a first top surface portion of a flat surface shape with a height equal to that of the middle step surface and a second top surface portion with a height equal to or higher than that of the first top surface portion, and a first electrode provided astride and above the first top surface portion of the first semiconductor layer and the middle step surface of the semi-insulating substrate. Instead, the '176 document shows only an upper and a lower step.

The '471 document teaches in Fig 2 that selective removal of the substrate down to the level of the first semiconductor layer allows the formation of an electrode, which is more stable and reliable (abstract). As can be seen in Fig 2, this selective removal of the substrate forms a middle step (top surface of item 3 on the right), and the first semiconductor layer ends up being level with the middle step. The lower step (bottom of item 5) is between the upper step (top of item 4) and middle step in a lateral direction. The first electrode (7) is formed astride and above the first top surface portion and the first semiconductor layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of the '471 document on the structure disclosed by the '176 document in order to form a reliable electrode on the first semiconductor layer.

6. Regarding claim **2**, the '176 document discloses in Fig 1(c) the photodetector of claim 1 further comprising a third semiconductor layer (3) formed between the first semiconductor layer (2) and the second layer (4) and having a carrier density lower (n-) than that of the first layer (p+) or the second layer (n).

7. Regarding claim **3**, the '176 document discloses in Fig 1(f) the photodetector according to claim 1 wherein a ramp portion consisting of a level difference between the upper step surface (4) and the middle step surface (top of item 2, which is level with substrate 1 when combined with the teachings of the '471 document) of the semi-insulating substrate is inclined in a radial direction of a depression formed by the upper step surface and the middle step surface, in a direction from the lower step surface to the upper step surface.

8. Regarding claim **4**, the '176 document discloses in Fig 1 a method of production of a semiconductor photodetector comprising: a first step of forming a recess with a predetermined depth in a semi-insulating substrate by etching (Fig 1b); a second step of forming a stack of a first semiconductor layer (2) comprising a first impurity and a second semiconductor layer (4) comprising a second impurity, selectively only in the recess of the semi-insulating substrate formed in the first step (Fig 1d);

The '176 document fails to disclose a third step of further etching a part of the semi-insulating substrate so as to expose at least a portion of the first semiconductor layer formed in the second step; and a fourth step of laying a first electrode in contact with the exposed portion of the first semiconductor layer exposed in the third step and laying a second electrode in contact with the second semiconductor layer above the semi-insulating substrate. Instead the '176 document shows in Fig 1e that the semiconductor layers are etched instead of the substrate in order to gain access to the first semiconductor layer.

The '471 document teaches in Fig 2 that selective removal of the substrate down to the level of the first semiconductor layer allows the formation of an electrode, which is more stable and reliable (abstract). As can be seen in Fig 2, this selective removal of the substrate forms a middle step (top surface of item 3 on the right), and the first semiconductor layer ends up being level with the middle step. The lower step (bottom of item 5) is between the upper step (top of item 4) and middle step in a lateral direction. The first electrode (7) is formed astride and above the first top surface portion and the first semiconductor layer. It would have been obvious to one of ordinary skill in the art at

the time of the invention to use the teachings of the '471 document on the structure disclosed by the '176 document in order to form a reliable electrode on the first semiconductor layer.

9. Regarding claim **5**, the '176 document discloses the method of claim 4, wherein the second step of forming the stack of first and second semiconductor layer is accomplished by vapor deposition (abstract).

10. Regarding claim **6**, the '176 document discloses the method of claim 4 wherein the first step is to form the recess of the semi-insulating substrate (Fig 1e) so that at least a side wall portion on the second electrode side (left sidewall of recess in item 1) among side wall portions in a sectional shape along a direction connecting the first electrode to the second electrode is of an inverted mesa shape.

Double Patenting

11. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

12. Claims **1 and 2** are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 3, respectively, of copending Application No. 10/864,797 (final numbered claims as noted in the Issue Classification of 11 July 2006). Although the conflicting claims are not identical, they are not patentably distinct from each other because:

13. Regarding instant claim **1**, claim 1 of the '797 application recites a semi-insulating substrate with upper, middle and lower regions, where the lower region is connected to the upper and middle regions (corresponds to an upper step, middle step and lower step, where the lower step is laterally between the upper and middle steps) The '797 application also recites a first semiconductor layer of a first impurity (p-type) provided on the lower region, having a first top surface on level with the middle region and a second top surface on level with or higher than the first top surface, and claims a second semiconductor layer formed above the first semiconductor layer and having a top surface on level with the upper region. Finally, the '797 application recites a first and second electrode, the first electrode astride (covering the boundary) the first semiconductor layer and middle region and the second astride the second semiconductor layer and upper region.

14. Regarding claim **2**, claim 3 of the '797 application recites each of the limitations of claim 1 as discussed above, and also recites a third semiconductor layer interposed between the second portion of the first semiconductor layer and the bottom surface of

the second semiconductor layer, the third semiconductor layer having a carrier concentration lower than those of the first and second semiconductor layers.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John C Ingham JCI

HOWARD WEISS
PRIMARY EXAMINER